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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,277	05/08/2001	Tae-Sung Jung	5649-894	3420

20792 7590 08/04/2005

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EXAMINER	
CHEN, ALAN S	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,277	JUNG ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Response to Arguments

1. Applicant's arguments filed 06/13/2005 have been fully considered but they are not persuasive.

2. Per claims 1 and 11 regarding the rejection using Adachi and Kaneco et al., applicant argues logic circuit 22 is part of the memory controller, sharing the 3V power supply with the lines 122 and 124 citing reference to Column 3 of Adachi. While Examiner does not deny the logic circuit 22 is a controller, the Examiner asserts element 10 is a memory controller as stated in the previous office action. It is clear by Adachi, that the processor generates the data goes into the memory, e.g., it is the source of the data, ultimately providing the data to the memory card 14 (Column 12, lines 46-50). Under the broadest reasonable interpretation of the claim language, one would deem the processor 10 as a memory controller, controlling what data that is written to the memory card. It is clear from FIGURE of Adachi that element 10, the memory controller, relies on a supply voltage (5V) that is separate and independent of the line voltage (3V) when the switch 26 is in a particular setting. The 3V setting operates the channel lines 122 and 124 independent of the 5V. Kaneco demonstrates the ability for the memory card to be independently powered and establishes the obviousness of claims 1 and 11. The rejection of dependent claims 2,3,5,12,13 and 15 are maintained.

3. Per claims 1 and 11 regarding the rejection using Suh, Merrit and Taguchi, Examiner believes the evidence of obviousness still remains on the claims in spite of applicants arguments. Applicant argues the lack of an independent voltage source for receiver 13 in Suh, the sharing of the transmission line voltage with the devices in Merrit and circuitry in Taguchi responsive to the same voltage (e.g., 2.5V).

Examiner does not agree, since Suh, Merritt and Taguchi are all along the same vein involving memory interface devices sharing a transmission medium, each disclosing an advantage in design that can obviously be incorporated with each other. Beginning with Suh, Suh clearly shows two independent chips (Fig. 3, element A and B) that show a transmission medium 12 powered by a terminal voltage, Vtt. While the differential amplifiers Suh uses in chip A and B does not explicitly show a power supply independent of Vtt, *it is* well-known to one of ordinary skill in the art that op-amps require an power independent of the input differential signals (see pg. 3 of attached *operation amplifier* definition from *Wikipedia*, e.g., a common source supply based off a BJT is Vcc). Depending on the necessary output signal of the operational amplifiers, a particular gain is required that is in large part dictated by the power supply (see page 3, DC Behaviour section of Wikipedia). It would appear restrictive if one were to limit the gain of the operational amplifier based on the voltage of a transmission path, e.g., Vtt for element 12, the op-amp, particularly if Vtt was used as an input to the differential opamp. Turning to Merritt inventions, Merritt relates to memory interfaces, particularly a memory controller 200 and memory 100 operating on separate chips 200 and 100, where each have their own independent power supply e.g., Vcc1 and Vcc2. The use of different power supplies is to ensure better performance, e.g., the requisite amount of power to operate the memory controller and another different amount of power to operate the memory since their hardware logic is different (Column 3, lines 60-67 and Column 4, lines 50-60). This clearly applies in the case of Suh, where chips A and B may comprise different logic. The reference to Taguchi strengthens the argument further showing independent power supplies, particularly between the terminal voltage and separate devices are beneficial, where Taguchi discloses adjusting power,

particularly to increasing Vtt of the transmission line, while keeping device 31 and 33 voltages the same, would yield better performance (e.g., Column 8, lines 4-10). Thus, having independent power supplies for the terminal voltage of the transmission line and each of the devices attached to it would allow more control and better performance of the entire system.

4. Per claims 10 and 20, applicant argues the lack of teaching in all the references regarding the terminal voltage having a magnitude greater than the magnitudes of the memory supply voltage and controller supply voltage.

As stated in the previous office action, Taguchi teaches generally that the higher the voltage supply the better the performance, e.g., in Taguchi's particular design, voltage above 2.5 V would enhance performance (Column 8, lines 5-10; also Column 8, lines 15-20 indicate Vtt not being limited to 2.5V and the respective tolerance voltage range).

5. The rejection of claims 1-20 is maintained and reiterated below.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-3,5,11-13,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of Kaneko et al.

The indicated claims are being rejected as being obvious over Adachi in view of Kaneko et al. First, turning to claim 1, it is to be noted that this claim only require a memory interface system with the channel line coupling the memory to the memory controller with the line being responsive to a terminal voltage that is independent of the other supplies. Please note, that the claim only requires a "responsive" without further defining this facet. Hence, turning to Adachi, one finds a memory card 14 that is either powered by a 3V or 5V source, with certainly the indication that the voltage source is contained in the memory card, as there is no supply passing from the camera 1 thereto, as the only connection points are the at least one channel lines 122,124 that couple the memory 14 to the memory controller 10, such that the at least one channel lines are responsive to either the 3V or 5V source of the camera. As the 3V and 5V sources of the camera 1 are shown to be independent as they are not connected nor shown to be of a common source, they are thus as independent as applicants have shown and claimed. Thus in a situation when the memory card 14 is supplied at a 3Vlevel, the switch 126 makes lines 122/124 and level shifter 20 and lines 114/112 responsive to the terminal voltage of the 3V camera supply, which is in turn independent of the camera's 5V supply. Note also that the rest of 16, not including level shifter 24, is also supplied by the 3V supply, thus making the terminal voltage, to which the channel lines 122/124 are responsive, independent of the 5V supply powering the memory controller 10. What is missing is evidence that memory card has its own independent supply, which would thus make the supplies of the memory, the memory controller and the channel lines independent, to the extent claimed.

Thus one of ordinary skill in the art is motivated to look for cameras with memory cards, to see how these cards are supplied. One example of such is Kaneko et al., in which one finds a camera 20 with its own supply 35 and a memory card 50 with its own built in battery 51. Please refer to the English language abstract and Figure 1, which clearly show the independent supplies of the memory and the camera.

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Adachi per the teachings of Kaneko et al. as Kaneko et al. have shown that it is old and well known in the art to supply a camera and its memory card via separate and independent power supplies. Thus in combination, when Adachi is operated with a memory card supplied by its own independent 3V source, as shown per Kaneko et al. to be independent, the channel lines 122/124 and the level shifter 20 and the logic circuit 22 are thus all powered by, and hence responsive to, the camera's 3V supply, which is also independent of the camera's 5V supply. Also note in Kaneko et al. that a plurality of independent supplies are shown in the camera at 35 and 37, which are also shown to be of differing voltages noting the conventional symbology for each battery. When the memory card is operable connected, the memory thus comprises the first receiver 21b and transmitter 21a in the level shifter 20, and the memory controller comprises also the second receiver 25a and transmitter 25b in the second level shifter, wherein at least one channel line 114/112 and 116/110, responsive to the 3V supply, serve to couple the first and second receivers/transmitters, per claim 2. Thus per claim 3, the first receiver/transmitter is powered by the 3V supply and the second receiver/transmitter is powered by the 5V supply that supplies the controller. While the 3V supply powering the first receiver/transmitter is in the camera, it is a mere substitution of supplies to power such via the memory card battery when it is operating at 3V, thus rendering such obvious. Turning to claim 5, the level shifters serve to provide a coupling function, with 20 coupling 124 to 21a to 114 to 116 and 20 coupling 110 to 112 to 21b to 122. Note that the breadth of the coupling allows for the references to meet what is claimed. As both references process data to the extent claimed, claims 11-13 and 15 are rejected for the same reasons.

10. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of Kaneko et al. as applied to claims 1-3,5,11-13,15 above, and further in view of Taguchi.

Turning to claims 10 and 20, the combined teachings of Adachi and Kaneko et al. lack the express teaching that the terminal voltage magnitude be greater than the others. Turning to Taguchi, one finds a similar setup in which the terminal voltage of the coupling line 10 is at 2.5V, the same level as the other sources. However, it is expressly taught at column 8, lines 4-9, that to increase the terminal voltage above 2.5V results in further enhanced performance, thus increasing the coupling line voltage to a value higher than used in the devices 20, which are memories and memory controllers. Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Adachi and Kaneko et al. per the teachings of Taguchi, so that the coupling lines are responsive to the highest voltage magnitude in order to further enhance performance.

11. Claims 4,6-9,14,16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of Kaneko et al. as applied to claims 1-3,5,11-13,15 above, and further in view of Taguchi.

Turning to claims 4,6-9,14,16-19, one finds that Adachi in view of Kaneko et al. lack the specifics of the transmitters and receivers. Turning to Suh, one finds that it is conventional in the art of memory bus interface circuits to use a coupling bus 12 that is responsive to a terminal voltage Vtt, with a transmitter 11 and receiver 13, wherein the receiver uses a reference voltage, and the transmitter is independent of other voltages as it driven at its gate and not supplied by a separate source, as it too is responsive to the terminal voltage (i.e. connected the same way as applicants' 102). Per column 1, the driver/transmitter is of the open drain structure and are MOS transistors. The receivers in the form of 13 are comparators per columns 1 and 2, wherein comparators are commonly made from differential amplifiers, per column 4. Note also that each receiver has a corresponding reference voltage and is responsive to the data carried on the coupling bus line, with the same type of connections as applicants have shown in their Figure 2. Advantages of Suh include things such as decreased common mode noise, influence of ground bounce, and the like per column 2, lines 30+, which parallel applicants' Figure 2 layout. Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the combined teachings of Adachi and Kaneko et al. per the teachings of Suh in order to include open drain transmitters and comparator/differential amplifier receivers in the memory and controller, so as to decrease common mode noise, influence of ground bounce. When combined, the transmitters and receivers of Suh would be placed in the level shifters of Adachi such that the transmitters are located in the memory to input to the level shifter 21a and in the controller to input to level shifter 25b, and the receivers to receive the data at 142 from 25a and at 122 to receive the data from 21b. Hence the level shifters serve to couple the discrete receivers as claimed.

12. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh in view of Merritt and Taguchi.

Additionally, the teachings of Suh and Merritt and Taguchi can be combined as follows, to render claims 1-20 as obvious. Suh, the primary reference, in Figures 3 and 5, shows receivers recA/B of the differential amplifier type comparator (see column 4) and MOS transistor open drain transmitter drivers (per Figure 1, also called open driver structure at column 2+) coupled via a channel line 12, wherein the channel line 12 is responsive to a terminal voltage Vtt. Use is in a high-speed memory interface per column 3, lines 43-47, but express mention of the memory and memory controller is lacking, noting that data is clearly sent and received from chip to chip. In Figures 3 and 5, there are two separate and distinct chips shown in outline form and these are connected by the channel line. As such, the Vtt comes from outside of each chip, and is thus "independent" of these chips. As a point of comparison, applicants, page 4, lines 15, states that the VTER may be supplied from an external voltage source, and the discussion of Figure 2, lines 10-15 of page 7, reveal that the supply voltages are independent (i.e. all one can gather from the applicants' Figure 2 is about the same as what Suh has shown, that being an "independent" voltage supply means to be from an area outside of the dashed lines encompassing the other chips) and that per page 8, independent supplies mean that VTER can be increased above the values of VDD1 and VDD2 in order to improve signal to noise ratio. Hence, alone Suh meets one of the tests of Vtt being "independent" in that the Vtt is shown to be "off chip" when compared to the chip outlines of Figures 3 and 5, thus being shown to be the same "independent" as applicants have shown, as far as being "off chip" is concerned. However, Suh does not expressly teach the other aspect of an "independent" Vtt, that being the ability to increase Vtt above the values used in the chips, as applicants have shown "independent" to mean an "electrical independence" per column 3, lines 12-15, and the "off chip" locations of VTERM

in the Figures. Turning to Merritt, one finds that the chips have their own independent power supplies. For example, 200 qualifies as a memory controller, 100 is the memory, and there is a line coupling the two for data transmission at VIN. Per column 3, lines 59+, one finds explicit teachings that the power supplies 30 and 230 for the respective sections 100 and 200 are independent and operate at different voltage levels. Hence, Merritt, when applied to Suh, sets forth that each chip will have its own independent supply, and thus since the Vtt is supplied form outside the two chips, the 3 power supplies are independent to the extent shown in applicants' Figures. Now turning to Taguchi, the final part of power supply independence is taught. Similar to both Suh and what applicants have set forth, there are devices 30 coupled to a bus 10, which bus 10 is supplied by VTT. Note that each device 30 includes an open drain driver 31 and an input buffer 33, which has also as an input, a reference voltage. As pointed out in an earlier discussion of Taguchi, the material spanning columns 7 and 8 set forth the "voltage magnitude independence" of Vtt by explicitly teaching the positive aspects of raising the level of Vtt above 2.5V, thus being above the power voltage of the devices running at 2.5V (as seen in Figure 9), with advantages to include a further enhancement in performance. Thus it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Suh by the teachings of Merritt and Taguchi in order to have an independent terminal voltage which results in further performance enhancements. Thus the limitations of claims 1,10,11,20 have been addressed, noting that the systems combined set forth a "data processing system". For claims 2 and 12, note that Suh sets forth that each chip has its own transmitters and receivers, with a transmitter connected to a receiver by a channel line that is responsive to the terminal voltage Vtt, as seen in Figures 3 and 5 wherein drvA1 is coupled to recB1 via 12 and drvBn is

coupled to recAn by another 12. Note also that Suh teaches use in a memory interface and Merritt teaches a memory coupled to a memory controller. Regarding claims 3 and 13, note that Merritt teaches that each chip has its own independent source. Regarding claims 4 and 14, the transmitters of both Suh and Taguchi are "independent" in so far as they are connected to the bus in the same manner as those of applicants. Regarding claims 5 and 15, Taguchi teaches a level shifter 51-54 at the input buffer 33, which is also in the form of a differential amplifier. See column 8, lines 26+ and the discussion of Figure 9. Since Taguchi teaches a level shifter at the input buffer of a device 30, then in combination, all devices with input buffers (i.e. receivers) would also be equipped with a level shifter, thereby rendering obvious the first and second circuits. Regarding claims 6 and 16, the open drain transmitters are taught by Suh and Taguchi. Regarding claims 7-9 and 17-19, both Suh and Taguchi teach the use of reference voltage input receivers/buffers made up from differential amplifiers. As such, they are responsive to the data carried on these lines, as well as the reference voltages, as Suh clearly shows such a setup in Figures 3 and 5. See also the details of Taguchi's Figure 9. Again, level shifters at the input buffers are seen in Taguchi's Figure 9, thus the addition of such to Suh's receivers, which are the equivalent of the input buffers, is obvious subject matter, in order to benefit from Taguchi's level shifter (per column 8, lines 50+), expressly for better detection of the high/low status of the input signal.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
07/28/2005

KIM HUYNH
PRIMARY EXAMINER
8/2/05